What is Claimed is:

[c1] An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; and

selectable circuit means for alteration of the soft error susceptibility of said dynamic logic gate.

[c2] The integrated circuit of claim 1, wherein said selectable circuit means alters the critical charge at said output node.

[c3] The integrated circuit of claim 1, wherein said selectable circuit means alters the susceptibility of said output node to soft errors.

[c4] The integrated circuit of claim1, wherein said dynamic logic gate is a domino gate.

[c5] The integrated circuit of claim 1, wherein said selectable circuit means includes a keeper circuit.

[c6] The integrated circuit of claim 5, where said keeper circuit comprises:

a first circuit portion which includes a first keeper device providing an initial level of critical charge to said output node, said first keeper device coupled to said output node and coupled to a feedback device; and

a second circuit portion which includes a second keeper device to increase the critical charge level of said output node, said second circuit portion adapted to enable said second keeper device in response to an immunity enable signal.

[c7] The integrated circuit of claim 5, where said keeper circuit comprises:

a keeper device providing a selectable critical charge to said output node, said keeper device coupled to said output node and coupled to a feedback device, said keeper device and a precharge device of said dynamic logic gate coupled to an output of a multiplexer, said multiplexer adapted to selectively couple said keeper device and said precharge device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of said multiplexer.

[c8] The integrated circuit of claim 5, where said keeper circuit comprises:

a keeper device providing a selectable critical charge to said output node, said keeper device coupled to said output node and coupled to a feedback device, said keeper device coupled to a output of a first multiplexer adapted to selectively couple said keeper device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of said first multiplexer; and

a second multiplexer adapted to selectively couple a precharge device of said dynamic logic gate to the same voltage supply that said keeper device is coupled to, in response to an immunity enable signal received on a control input of said second multiplexer.

[c9] The integrated circuit of claim 1, further including:

a keeper circuit providing a critical charge to said output node, said keeper device coupled to said output node and coupled to a feedback device; and

a body bias circuit, said body bias circuit adapted to selectively alter the susceptibility of input devices of said dynamic logic gate to radiation events.

[c10] The integrated circuit of claim 9, wherein said body bias circuit includes a multiplexer adapted to selectively couple said bodies of said input devices to one of two or more biasing voltages in response to an immunity enable signal received on a control input of said multiplexer.

[c11] An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected; and

a keeper circuit adapted to selectively alter the critical charge of said dynamic logic gate.

[c12] The integrated circuit of claim 11, where said keeper circuit comprises:

a first circuit portion which includes a first keeper device providing an initial level of critical charge to said output node, said first keeper device coupled to said output node and coupled to a feedback device; and

a second circuit portion which includes a second keeper device to increase the critical charge level of said output node, said second circuit portion adapted to enable said second keeper device in response to an immunity enable signal.

[c13] The integrated circuit of claim 12, wherein said immunity enable signal is generated dynamically or is fixed during manufacture of said integrated circuit.

[c14] The integrated circuit of claim 11, where said keeper circuit comprises.

a keeper device providing a selectable critical charge to said output node, said keeper device coupled to said output node and coupled to a feedback device, said keeper device and a precharge device of said dynamic logic gate coupled to an output of a multiplexer, said multiplexer adapted to selectively couple said keeper device and said precharge device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of said multiplexer.

[c15] The integrated circuit of claim 14, wherein said immunity enable signal is generated dynamically or is fixed during manufacture of said integrated circuit.

[c16] The integrated circuit of claim 11, where said keeper circuit comprises:

a keeper device providing a selectable critical charge to said output node, said keeper device coupled to said output node and coupled to a feedback device, said keeper device coupled to an output of a first multiplexer adapted to selectively couple said keeper device to one of two or more voltage supplies in response to an immunity enable signal received on a control input of said first multiplexer; and

a second multiplexer adapted to selectively couple a precharge device of said dynamic logic gate to the same voltage supply that said keeper device is coupled to in response to an immunity enable signal received on a control input of said second multiplexer.

[c17] The integrated circuit of claim 16, wherein said immunity enable signal is generated dynamically or is fixed during manufacture of said integrated circuit.

[c18] An integrated circuit comprising:

a dynamic logic gate having an output node at which a logical output value of the logic gate is detected;

a keeper circuit providing a level of critical charge to said output node; and

a body bias circuit, said body bias circuit adapted to selectively alter the bias voltage applied to the bodies of input devices of said dynamic logic gate.

[c19] The integrated circuit of claim 18, wherein said keeper circuit comprises a keeper device coupled to said output node and coupled to a feedback device.

[c20] The integrated circuit of claim 18, wherein said body bias circuit comprises a multiplexer adapted to selectively couple said bodies of said input devices of said dynamic logic gate to one of two or more biasing voltages in response to an immunity enable signal received on a control input of said multiplexer.